Master's Thesis

Thickness-Dependent Transport and Gate-Tunable Rectification in $PdSe_2$ Field-Effect Transistors

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2020

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A thesis/dissertation
submitted to the Graduate School of UNIST
in partial fulfillment of the
requirements for the degree of
Master of Science

Dongwook Seo

12/04/2019 of submission
Approved by

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Abstract

Two-dimensional materials such as Graphene and MoS_2 provide an ideal platform to realize extremely thin body metal-oxide-semiconductor field effect transistors (MOSFETs) which is highly immune to short channel effects in the ultra-scaled regime. Even with the outstanding carrier mobility in Graphene, however, Graphene's zero band gap limits practical electronic application. One of the transition metal dichalcogenides (TMDs), MoS_2 is also a popular two-dimensional material which has widely tunable band gap from ~1.9 eV at monolayer to ~1.2 eV at bulk MoS_2. In this work, we introduce one of the transition metal dichalcogenides, $PdSe_2$, which has been studied recently. We report theoretical studies on the thickness-dependent electronic properties of $PdSe_2$ and their effects on $PdSe_2$ field effect transistors through experimental demonstrations. Density functional theory calculations show that the band gap of $PdSe_2$ decreases from ~1.1 eV to ~0.3 eV as layer number increases from monolayer to bulk. We fabricate field effect transistors with different thicknesses of uniform $PdSe_2$ flakes on silicon substrate with 300 nm SiO_2 layer and characterize the thickness-dependent transport properties of $PdSe_2$ field effect transistors. Furthermore, we fabricate field effect transistors using nonuniform $PdSe_2$ flake composed of thin and thick regions which show rectification behavior like diode. One interesting finding is that the rectification direction can be controlled by gate voltage. This gate-tunable rectification in heterojunction $PdSe_2$ field effect transistors can be understood through energy band diagram alignment analysis. To achieve gate-tunable rectification, proper combination of $PdSe_2$ flakes with different thicknesses is required since the energy band alignment at the heterojunction is critical.

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Nomenclature

MOSFETs	Metal-oxide-semiconductor field effect transistors
TMDs	Transition metal dichalcogenides
DFT	Density functional theory
GGA	Generalized gradient approximation
CBM	Conduction band minimum
VBM	Valence band minimum
BZ	Brillouin zone
OM	Optical microscope
AFM	Atomic force microscopy
PDMS	Polydimethylsiloxane
BD	Band diagram

I. Introduction

For the last few years, two-dimensional materials such as Graphene and MoS_2 have been widely explored for the future electronic device applications [1-3]. Graphene has gained big attention due to its high carrier mobility, but zero band gap of Graphene limits electronic application [1]. Gapped two-dimensional materials, represented by transition metal dichalcogenides such as MoS_2, are attractive candidates for the channel materials in highly scaled MOSFETs since their extremely thin thickness allows almost ideal electrostatic control on the channel and makes it robust to short channel effects [2-8]. Transition metal dichalcogenides are composed of transition metal and chalcogen atoms, and the ratio of the number of atoms is literally 1:2. A lot of two-dimensional transition metal dichalcogenides monolayers have sizable band gap which is generally in the range of 1 eV to 2 eV, and the band gap decreases as the number of layer increases. Some two-dimensional materials have zero band gap in the bulk while others have non-zero band gap. This decreasing band gap trend is the common property for two-dimensional materials, which results from the interactions between layers [9,10]. This thickness-dependent band gap is the unique property which is not observed in conventional semiconductor materials. We focus on $PdSe_2$, one of the transition metal dichalcogenides, which has been studied recently.

II. Results and Discussion

2.1. Crystal Structures of Monolayer and Bulk $PdSe_2$

We first study band structures of monolayer and multilayer $PdSe_2$ through density functional theory (DFT) using Atomistix Toolkit (ATK) [11-13]. We employ generalized gradient approximation (GGA) and Perdew-Burke-Ernzerhof (PBE) functionals to represent exchange-correlation potentials for geometry optimization and band structure calculations [14].

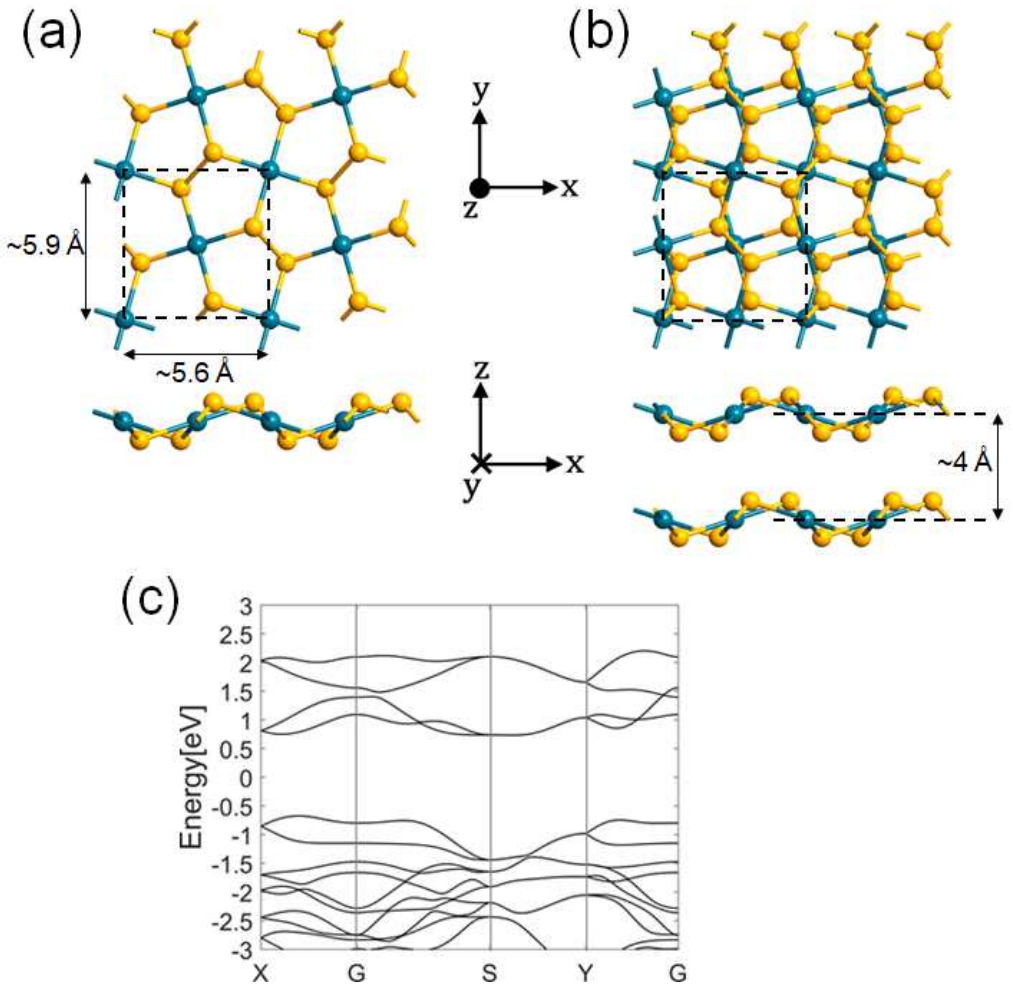


Figure 1. (a) Top and side views of monolayer $PdSe_2$. Dotted rectangle is primitive unit cell of monolayer $PdSe_2$. (b) Top and side views of bulk $PdSe_2$. Dotted rectangle is primitive unit cell of bulk $PdSe_2$. (c) Band structures of monolayer $PdSe_2$ along the path X-G-S-Y-G in 1st BZ. VBM point is located on X-G path, but CBM point is not located on the high symmetry path.

As in Figure 1a, monolayer $PdSe_2$ crystal structure is puckered pentagonal configuration. Two-dimensional materials with puckered pentagonal structure are highly desirable two-dimensional materials due to the low symmetry lattice structure. They have recently been predicted but remained unexplored experimentally [15-17]. Primitive unit cell of monolayer $PdSe_2$ is rectangular with the in-plane lattice constant a_x = ~5.6 Å, a_y = ~5.9 Å and the vertical puckering distance d = ~1.6 Å. These lattice constants are in good agreement with the other reported values [18,19]. Figure 1b shows the unit cell of bulk $PdSe_2$, which is staggered vertical superposition of two adjacent monolayers. The vertical distance between two monolayers is ~4 Å and the unit cell of bulk $PdSe_2$ is orthorhombic unit cell. Electronic band structure for monolayer $PdSe_2$ is calculated and plotted along the high symmetric path for the 1st Brillouin Zone (BZ), X-G-S-Y-G path in Figure 1c. The valence band maximum (VBM) point is located on X-G path. Interestingly, the conduction band minimum (CBM) point is not located on the X-G-S-Y-G path. Therefore, the electronic band structure on the specific path for the 1st Brillouin Zone is not enough and energy contour plots for the lowest conduction band and the highest valence band on whole 1st Brillouin Zone are required to understand the electron and hole carriers in monolayer $PdSe_2$.

2.2. Band Structures of $PdSe_2$

Figure 2a,b show energy contour plots of the lowest conduction band and highest valence band in monolayer $PdSe_2$, respectively. In Figure 2a, the conduction band minimum point is confirmed to be close to the S-Y path as indicated by the dotted circle in the energy contour plot. The first quadrant of the lowest conduction band energy contour plot is magnified and shown in Figure 2c. The dotted elliptical shape represents the shape for conduction band minimum valley, which is anisotropic. Two arrows mean k-space vectors for heavy and light effective mass, and the heavy effective mass m_H = ~1.4 electron mass and the light effective mass m_L = ~0.5 electron mass are calculated from energy values around the conduction band minimum point. This means monolayer $PdSe_2$ has four anisotropic valleys in the 1st Brillouin Zone for electron carriers on the lowest conduction band. The anisotropic shape valleys for electron and hole carriers result from the low symmetry and puckered pentagonal atomic structure of $PdSe_2$ monolayer [20].

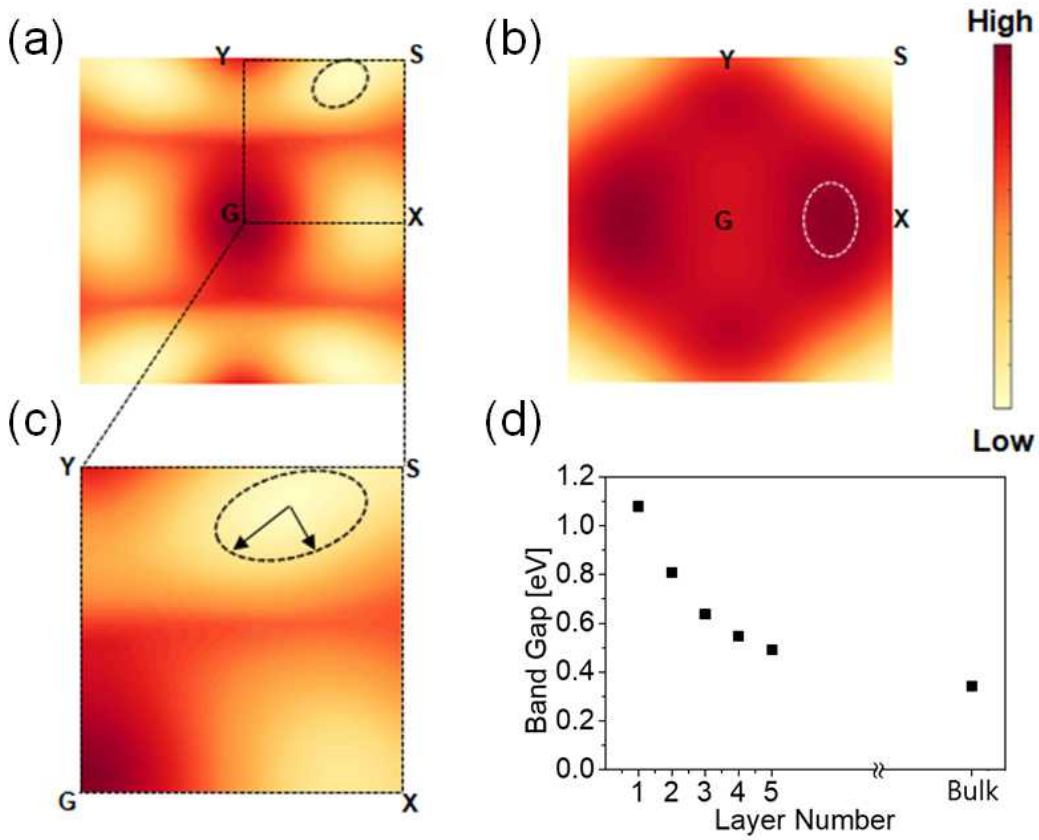


Figure 2. (a) Energy contour plots of the lowest conduction band in monolayer $PdSe_2$. Dotted circle indicates CBM region. (b) Energy contour plots of the highest valence band in monolayer $PdSe_2$. Dotted circle indicates VBM region. (c) First quadrant for energy contour plots of the lowest conduction band. (d) Computed band gap values depending on the layer number of $PdSe_2$.

The band gap values for monolayer to pentalayer and bulk $PdSe_2$ are calculated through DFT using GGA and PBE functionals. The band gap values as a function of $PdSe_2$ layer number is shown in Figure 2d. This figure shows a clear decreasing band gap trend from ~1.1 eV (monolayer) to ~0.3 eV (Bulk). There are other studies that report different band gap values, especially zero band gap for bulk $PdSe_2$ [20]. In general, band gap value predicted by DFT is strongly dependent on simulation conditions. We have checked that bulk $PdSe_2$ has non-zero band gap experimentally, and it is discussed in the next electrical measurement part.

2.3. Uniform Thickness $PdSe_2$ Field Effect Transistors

To understand the thickness-dependent transport properties of $PdSe_2$, we fabricate more than 20 back-gated field effect transistors using various thicknesses of uniform $PdSe_2$ flakes as the channel material. Mechanical exfoliation using Scotch tape and polydimethylsiloxane (PDMS) is used to get the $PdSe_2$ flakes on SiO_2 surface. The used substrate is heavily doped p-type Si with 300 nm SiO_2 layer on the doped Si. Cleaning process with acetone and isopropyl alcohol is conducted after getting $PdSe_2$ flakes through exfoliation method. Annealing process for two hours at temperature ~523 K is conducted to remove unnecessary residue from tape and chemical residue. Using optical microscope, uniform $PdSe_2$ flakes with various thicknesses are found. After finding proper uniform $PdSe_2$ flakes, atomic force microscopy (AFM) measurement is conducted to estimate the exact thickness information for the $PdSe_2$ flakes. After getting the thickness information, we select good $PdSe_2$ flake with proper thickness and the electron-beam lithography is followed to pattern the source and drain contact electrodes. The electron-beam evaporation is used to make source and drain contact electrodes. In our fabrications, Ti 10 nm layer for adhesion layer and Au 50 nm layer on Ti layer are deposited by the metal deposition process. At room temperature and atmospheric pressure condition, electrical characteristics are measured using Keysight B1500A semiconductor parameter analyzer.

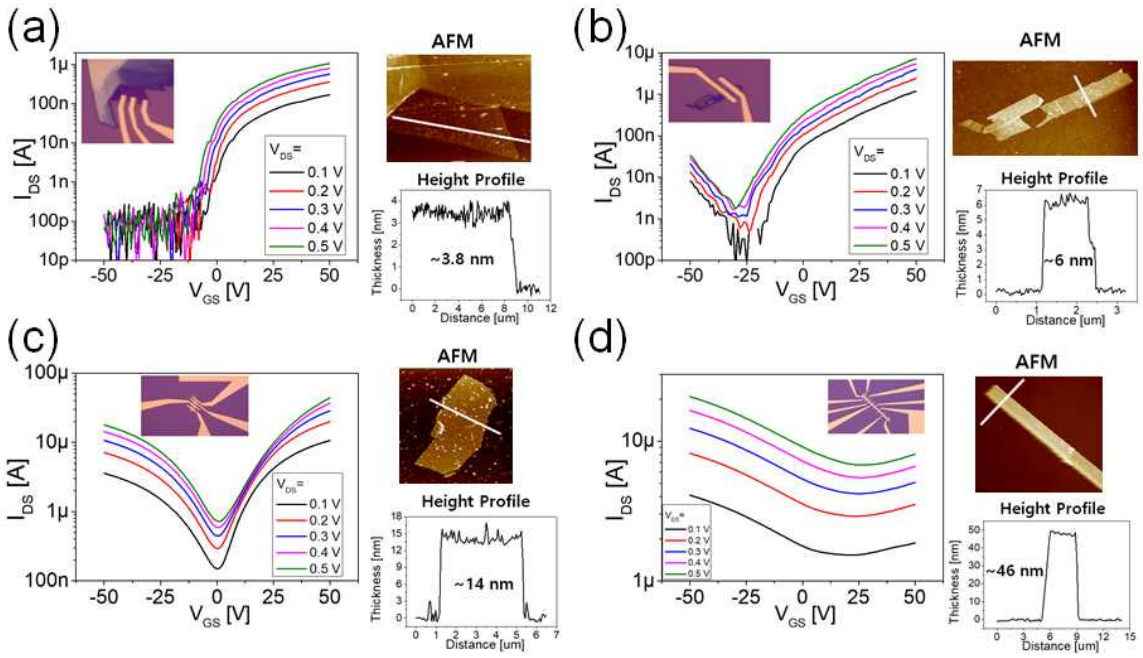


Figure 3. Transfer I-V curves, OM images, AFM images and channel $PdSe_2$ flake height profiles for devices. (a) Thickness is ~3.8 nm. High On/Off ratio and n-type characteristics are observed. (b) Thickness is ~6 nm. There is no flat region in transfer I-V curves. (c) Thickness is ~14 nm. Ambipolar characteristics is observed. (d) Thickness is ~46 nm. Small gating and semi p-type characteristics is observed.

Figure 3a-d show the four representative uniform thickness $PdSe_2$ flake channel devices. The transfer I-V curves for the devices are measured in the range of -50 V to 50 V with 10 V step for V_{GS} and in the range of 0.1 V to 0.5 V with 0.1 V step for V_{DS}. The optical microscope images for the devices, and atomic force microscope images for the $PdSe_2$ flakes with height profile on the black or white line in AFM image are provided with the transfer I-V curves. The channel $PdSe_2$ flake thicknesses are about 3.8, 6, 14 and 46 nm for Figure 3a-d devices, respectively. According to the height profiles, the $PdSe_2$ flakes have quite uniform thickness.

As $PdSe_2$ flake thickness increases, from Figure 3a to Figure 3d, On current and Off current increase and the On/Off ratio decreases. In general, the channel resistance is inversely proportional to channel thickness, thus On current and Off current should be proportional to the channel thickness if the channel material is normal material. However, since $PdSe_2$ has decreasing band gap as material thickness increases, sharply increasing current level can be seen from Figure 3a to Figure 3d. Transfer I-V curve has a flat region when V_{GS} is negative in Figure 3a, and then as flake thickness increases, that flat region in I-V curve disappears and hole current starts to increase as seen in Figure 3b-d. If $PdSe_2$ flake thickness is thin enough, n-type characteristics can be seen like I-V curves in Figure 3a. As flake thickness increases, ambipolar characteristics is observed in Figure 3c. When flake thickness becomes very thick in Figure 3d, the I-V curves show semi p-type characteristics. One important result is that small gating exists in the transfer curves in Figure 3d. This means ~100 layers of $PdSe_2$ flake have non-zero band gap. Since 100 layers of two-dimensional material can be considered as a bulk material, these experimental results suggest non-zero band gap in bulk $PdSe_2$, which is consistent with the non-zero band gap value in bulk in Figure 2d.

2.4. On/Off Ratio and Maximum Mobility Distribution

Figure 4 shows measured On/Off ratio and maximum mobility distribution as a function of $PdSe_2$ flake thickness for more than 20 back-gated $PdSe_2$ field effect transistors. In Figure 4a, clearly decreasing band gap trend is observed as $PdSe_2$ flake thickness increases. These On/Off ratio values are measured on the positive V_{GS} region from the minimum current point, which means those On/Off ratio values are for electron current. As mentioned previously about Figure 3a-d, normally thin $PdSe_2$ has n-type characteristics, and as flake thickness increases, it becomes ambipolar and p-type. Transfer I-V curves measured from devices made of $PdSe_2$ flake thicker than ~20 nm normally show semi p-type characteristics. Thus measured data from $PdSe_2$ field effect devices made of $PdSe_2$ flake thicker than ~17nm are not included in the Figure 4a,b.

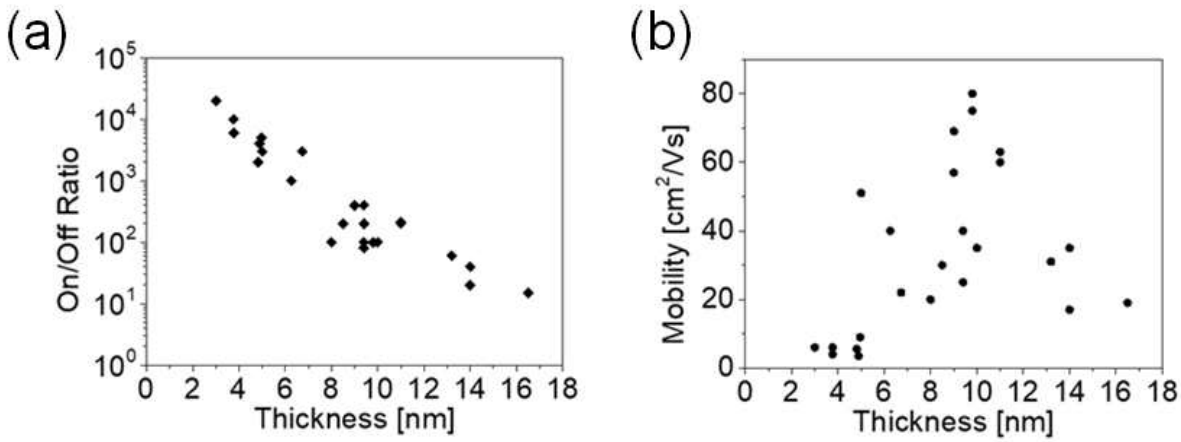


Figure 4. (a) Calculated On/Off ratio values from transfer I-V curves for uniform thickness $PdSe_2$ field effect transistors. On/Off ratio distribution shows decreasing trend as flake thickness increases. (b) Calculated maximum mobility distribution for uniform thickness $PdSe_2$ field effect transistors. Around 10 nm thickness flake has higher mobility value.

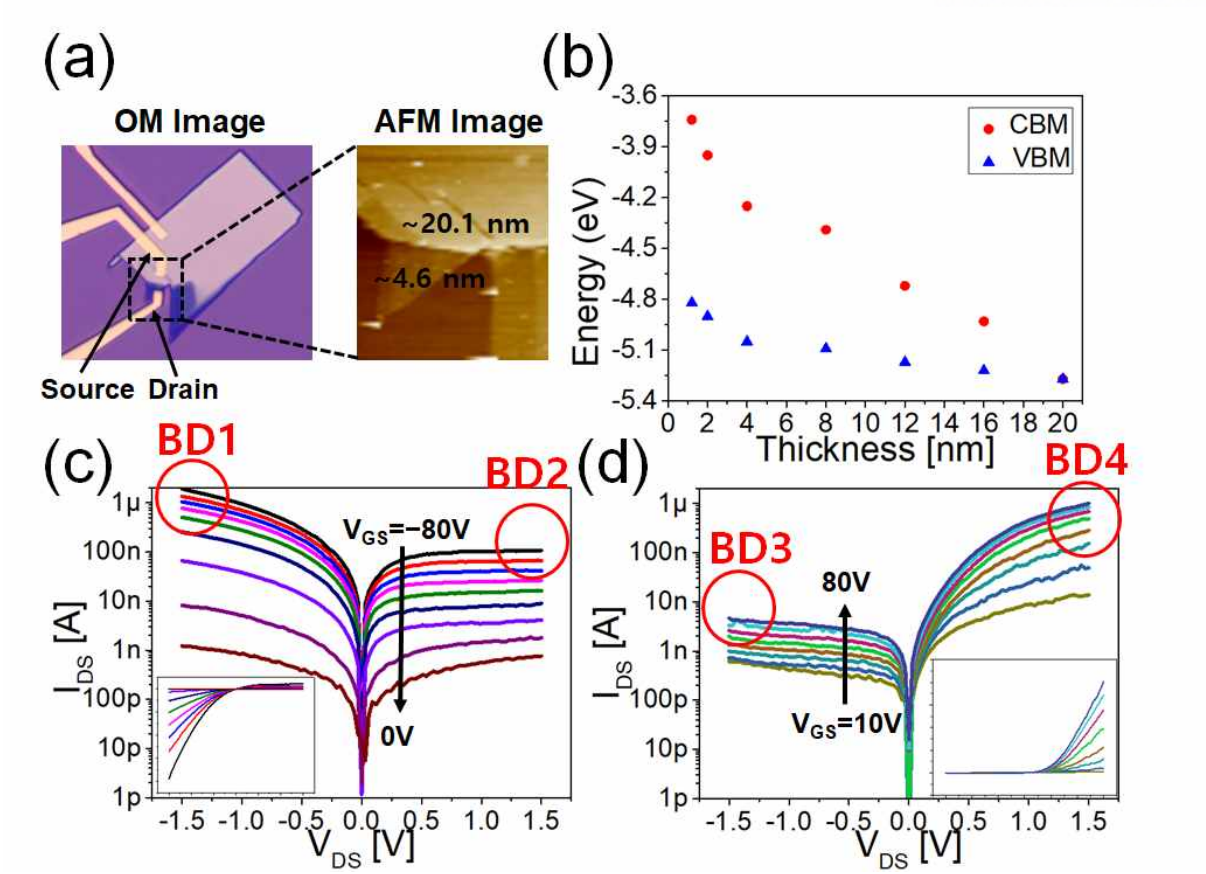
The thinnest $PdSe_2$ flake thickness used in our devices is ~3 nm and the measured On/Off ratio is ~20000. As flake thickness increases, the band gap of $PdSe_2$ flake decreases and the decreased band gap results in decreasing On/Off ratio in Figure 4a. This experimental result is consistent to the decreasing band gap trend from simulation work in Figure 2d. Our experimental electron mobility values are similar or a little lower than other study's reported values [20]. In the measured mobility distribution Figure 4b, $PdSe_2$ flakes of around 10 nm thickness have the highest mobility value. For thin flakes (< 9 nm), the charge screening is insufficient, resulting in the lower mobility. As the layer number increases, mobility is generally enhanced due to the screening. However, at the same time, an additional interlayer resistance is imposed for the thicker $PdSe_2$ FETs since source and drain contacts are directly connected only to the top $PdSe_2$ in this back-gated FETs. Therefore, if flakes become thicker than ~10

nm, mobility degradation by the interlayer resistance dominates the mobility gain from the charge screening [21].

2.5. Device Structure and Output I-V Curves of $PdSe_2$ Heterostructure Field Effect Transistor (Device 1)

To understand the thickness-dependent transport more deeply, we fabricate other type devices using heterostructure $PdSe_2$ flakes. Mechanical exfoliation using Scotch tape and polydimethylsiloxane (PDMS) is used to get the $PdSe_2$ flakes on SiO_2 surface. Cleaning process with acetone and isopropyl alcohol is conducted after getting $PdSe_2$ flakes through exfoliation method. Annealing process for two hours at temperature ~523 K is conducted to remove unnecessary residue from tape and chemical residue more clearly. Using optical microscope, heterostructure $PdSe_2$ flakes which have two different thickness parts are found as seen in the OM image of Figure 5a. After finding some proper heterostructure $PdSe_2$ flakes like the one in Figure 5a, atomic force microscopy (AFM) measurement is conducted to know the thickness for the both thin and thick sides of the heterostructure $PdSe_2$ flake. After getting the thickness information for heterostructure $PdSe_2$ flaks, we choose several good heterostructure flakes. The electron-beam lithography is used to pattern the source and drain contact electrodes. Then, source and drain contact electrodes are made by the electron-beam evaporation. In our fabrications, Ti 10 nm layer for adhesion layer and Au 50 nm layer on Ti layer are made by the metal deposition process. At room temperature and atmospheric pressure, electrical characteristics are measured using Keysight B1500A semiconductor parameter analyzer.

There are OM image for the fabricated heterostructure $PdSe_2$ field effect transistor (Device 1) in Figure 5a, and AFM image for the heterostructure $PdSe_2$ flake which is used in the device in Figure 5b. As in the AFM image of Figure 5b, the thin side of 4.6 nm thickness part is set to drain, and the thick side of 20.1 nm thickness part is set to source. Therefore, between the source electrode and the drain electrode, there is the $PdSe_2$ flake channel which has two different thickness parts. The measured V_{DS} range is from -1.5 V to 1.5 V, and the V_{GS} range is from -80 V to 80 V with the steps of 10 V. Figure 5c,d show the measured output I-V curves with the V_{DS} and V_{GS} range. The I-V curves are drawn with log scale for the I_{DS}, and small inset I-V curves are drawn with linear scale for the I_{DS}. Figure 5c is the output I-V curves for negative V_{GS} range from -80 V to 0 V, and Figure 5d is for positive V_{GS} range from 10 V to 80 V.



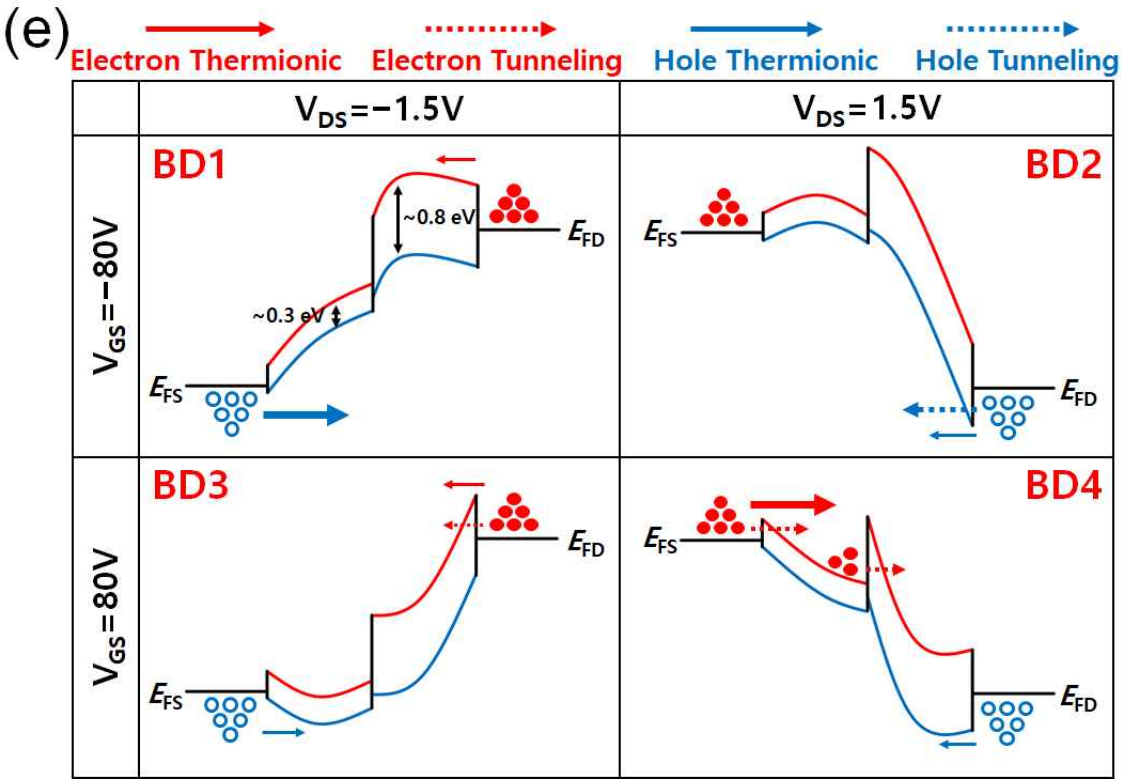


Figure 5. (a) OM and AFM images for Device 1. Heterostructure $PdSe_2$ flake is used as channel. (b) Experimentally reported CBM and VBM energy values as a function of $PdSe_2$ flake thickness. (c) Output I-V curves for Device 1 when V_{GS} is from -80 V to 0 V. (d) Output I-V curves for Device 1 when V_{GS} is from 10 V to 80 V. (e) Energy band diagram analysis to understand gate-tunable rectification behavior in Device 1.

In Figure 5c, clear rectification behavior is shown. When V_{GS} is negative near -80 V, the current level at negative V_{DS} is higher than the current level with positive V_{DS}. The current continuously increases for the negative voltage direction when V_{DS} is negative. However, with positive V_{DS}, the current is relatively low and does not increase even though V_{DS} continuously increases. We observe the current saturation when V_{DS} is positive. Therefore, this I-V curves show clear rectification behavior like a diode. It is easier to see the rectification behavior in the linear scale I-V curves in the inset of Figure 5c. On the other hand, the I-V curves for the positive V_{GS} also show rectification as we can see in Figure 5d. One interesting finding is that this current rectification direction becomes completely opposite when V_{GS} is positive. The current level is continuously increasing when V_{DS} is positive. However, when V_{DS} is negative, the current does not easily increase with the higher V_{DS} in the negative direction. This current rectification behavior is also more easily seen in the linear scale I-V curves in the inset of Figure 5d. This $PdSe_2$ heterostructure field effect transistor shows rectification behavior, and the rectification direction can be controlled by the V_{GS}, which has big merit compared to the other reported gate-tunable diode device [22].

2.6. Energy Band Diagram Analysis on Gate-Tunable Rectification

By using energy band diagram alignment analysis, we can understand the reason why this heterostructure device shows gate-tunable rectification behavior. To draw band alignment between thin and thick $PdSe_2$ flakes, we use experimentally measured CBM and VBM values of $PdSe_2$ flakes for various thicknesses [23]. Figure 5b shows the energy values of CBM and VBM as a function of number of $PdSe_2$ layers, which is taken from the other study [23]. The $PdSe_2$ heterostructure flake has two regions with different thicknesses. The thin region of ~4.6 nm thickness is ~11 layers of $PdSe_2$, and the corresponding band gap size is ~0.8 eV. The thick part of ~20 nm thickness is ~45 layers of $PdSe_2$, and the band gap size is ~0.3 eV. Using the values of CBM, VBM, and the band gap sizes, the four energy band diagrams are plotted in Figure 5e. Each band diagram in Figure 5e corresponds to each output I-V curve at specific V_{DS} and V_{GS}. The BD1,2,3,4 in Figure 5e correspond to the BD1,2,3,4 bias condition in Figure 5c,d, respectively. In Figure 5e, E_{FS} and E_{FD} is the fermi level of source and drain electrode, respectively. The conduction band color is red and valence band color is blue. The red small circles mean electron carriers, and the blue small circles mean hole carriers in source or drain electrode. The solid and dotted arrows represent thermionic emission and tunneling currents, respectively. The red arrows mean electron flow and the blue arrows mean hole flow from source or drain electrode. The size of the arrow is for presenting the magnitude of carrier flow. The specific bias conditions, which is V_{DS} = -1.5 V or 1.5 V and V_{GS} = -80 V or 80 V, are the extreme bias conditions in the measured V_{DS} and V_{GS} range.

As we can see in band diagram 1 figure (BD1), there is band gap difference between thin flake part and thick flake part. Also, as we can see in Figure 5b, since both CBM and VBM locations decrease as $PdSe_2$ flake thickness increases, staggered band gap is formed at the interface between the thick and thin energy bands. Since there is large enough energy barrier for the electrons at drain side, only small and negligible electron thermionic emission contributes to the total current. At source side, since there is very small energy barrier for holes, big hole thermionic emission and tunneling current can flow from source to drain. Therefore, the current in BD1 case mainly comes from hole flow from source to drain. The BD2 case is also analyzed in the similar way. In BD2, electron flow from source to drain is negligible because there is large energy barrier in the channel. At drain, some hole current can flow from drain to source by thermionic emission and tunneling. However, since the barrier size for holes at drain in BD2 is larger than the barrier size for holes at source in BD1, there is current level difference between BD1 region and BD2 region in Figure 5c. Since the barrier size for hole at BD2 drain is large enough, hole tunneling current is less than hole thermionic emission current and not easily increased by increasing V_{DS}. Therefore, we can see saturation of current in BD2 region in Figure 5c. As a result, we

can see the reverse rectification behavior with negative V_{GS}.

The rectification behavior when V_{GS} is near 80 V can be also understood through band diagram alignment analysis in Figure 5e. In BD3 case, there is not small energy barrier for holes at source. At the same time, there is also not small barrier for electrons at drain. Small hole thermionic emission, and small electron thermionic emission and tunneling flow from drain contributes to the total current. Therefore, the total current amount is minimized and current level in BD3 case is the smallest one among BD1 ~ BD4 case current level. However, one different thing to BD2 case is that BD3 case current is slowly increasing. In BD3 band diagram, hole thermionic emission flow from source is directly affected by V_{DS} magnitude. Therefore, BD3 case current is not perfectly saturated and slowly increasing as V_{DS} magnitude increases for the negative voltage direction. BD4 band diagram shows the last case when V_{GS} = 80 V and V_{DS} = 1.5 V. Since there is large energy barrier for holes, only small hole thermionic emission contributes to the total current. At source side, since there is small energy barrier for electron current, relatively large electron flow contributes to the total current. Therefore, BD4 region in Figure 5d shows higher current level than the current of BD3 case. There is second energy barrier for electrons in the BD4 case. Since this second energy barrier is thinned down by the high V_{GS}, electrons from the source can tunnel through the barrier to drain. However, even though this second barrier is very thin, it still imposes additional resistance in channel. Thus, the current level for BD1 is higher than the current level for BD4. As a result, we can see the forward rectification behavior with the positive V_{GS}.

2.7. Rectification Ratio in $PdSe_2$ Heterostructure Field Effect Transistor (Device 1)

It is observed that device 1 has rectification behavior like a diode. In output I-V curves, one side current is nearly saturated, and the other side current continuously increases. The rectification ratio is calculated and plotted in Figure 6a-c. In one output I-V curve in Figure 5c,d, $I_{Forward}$ and $I_{Reverse}$ can be defined. In output curve of Figure 5c, current when V_{DS} is negative is defined as $I_{Forward}$, and current when V_{DS} is positive is defined as $I_{Reverse}$. In output curve of Figure 5d, current when V_{DS} is negative is defined as $I_{Reverse}$, and current when V_{DS} is positive is defined as $I_{Forward}$. Using I_{DS} current values at positive $+V_{DS}$ and I_{DS} current value at negative $-V_{DS}$, the current rectification ratio $I_{Forward}$ / $I_{Reverse}$ is calculated. Figure 6a shows rectification ratio as a function of absolute V_{DS} value when V_{GS} is in the range from -80 V to -40 V. Figure 6b shows rectification ratio when V_{GS} is in the range from -30 V to 0 V. Figure 6c shows rectification ratio when V_{GS} is in the range from 10 V to 80 V.

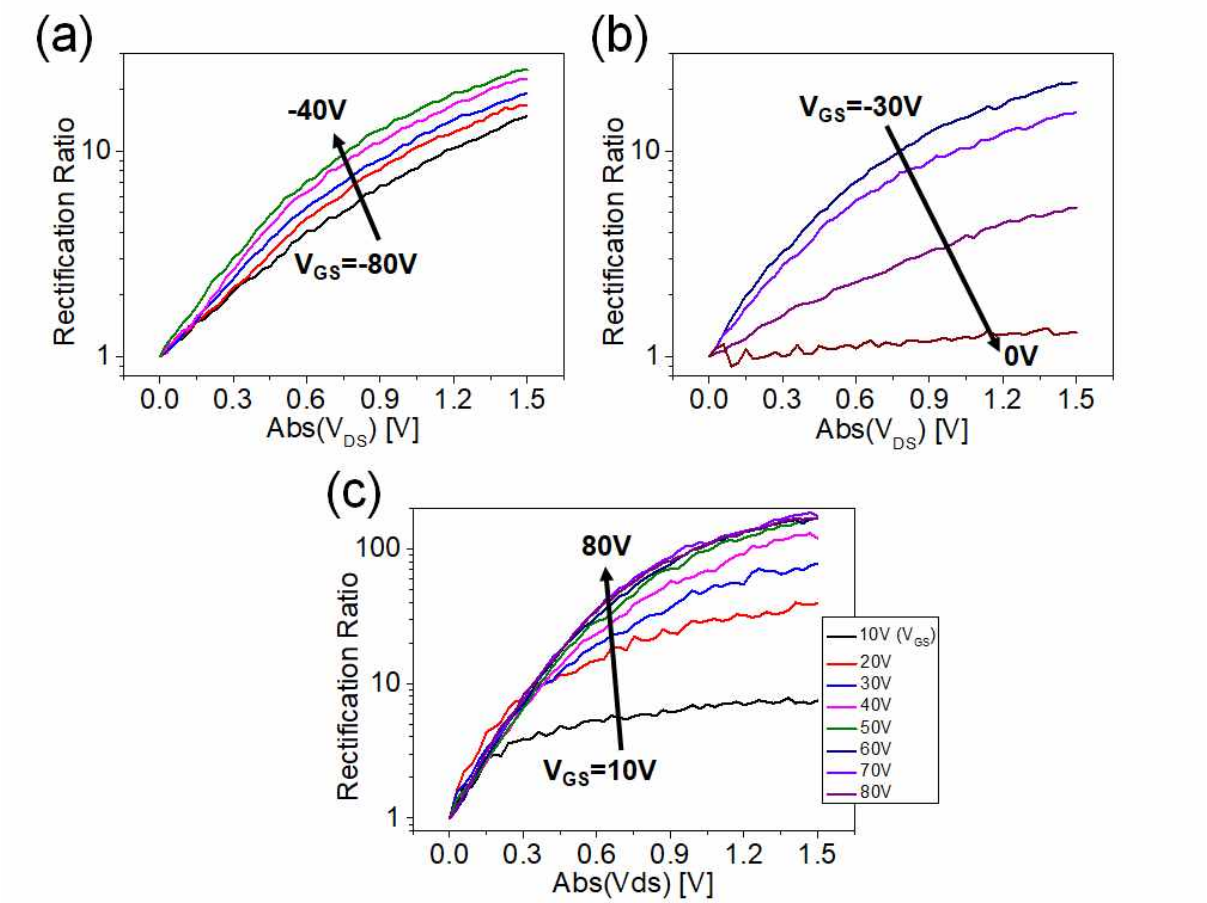


Figure 6. Current rectification ratio curves from output I-V curves for Device 1. (a) Rectification ratio increases from V_{GS} = -80 V to -40 V. (b) Rectification ratio decreases from V_{GS} = -30 V to 0 V. (c) Rectification ratio increases from V_{GS} = 10 V to 80 V. These (a), (b) and (c) curves show monotonically increasing rectification ratio curves as absolute V_{DS} increases from 0 V to 1.5 V.

Figure 6a shows that rectification ratio is monotonically increasing as absolute V_{DS} increases as V_{GS} increases from -80 V to -40 V. The rectification ratio monotonically decreases as V_{GS} increases from -30 V to 0 V in Figure 6b. The rectification ratio becomes the highest value when V_{GS} is -40 V and further increase of V_{GS} results in decrease of rectification ratio. The increase of V_{GS} results in energy band bending in BD1 and BD2 band diagram in Figure 5e. Even though the hole flow from source to drain increases, since the energy band bending in BD2 directly affect the energy barrier width for holes at drain, hole tunneling current also increases as a result of band bending. From -40 V to -80 V for V_{GS}, since the increase proportion in total current is higher in BD2 case, rectification ratio becomes highest when V_{GS} is ~40 V.

When V_{GS} is positive from 10 V to 80 V, the current rectification ratio curve looks monotonically increasing as V_{GS} increases. It is found that the rectification ratio monotonically increases when V_{GS} range is from 10 V to 50 V, and it becomes saturated when V_{GS} range is from 50 V to 80 V. When higher V_{GS} is applied as in BD3, electron current at drain increases but hole current decreases at source. This decreasing hole current results in small increase proportion of total current in BD3 region in Figure 5d compared to the BD2 region case in Figure 5c. This small increase proportion results in monotonic increasing trend of rectification ratio in Figure 6c. As V_{GS} becomes higher over 50 V, the increase proportion in total current in BD3 case increases since further energy band bending in BD3 results in big increase of electron tunneling current at drain. Therefore, the rectification ratio curve becomes almost saturated when V_{GS} is higher than ~50 V. It is also found that the rectification ratio value when V_{GS} is positive is generally higher than the case when V_{GS} is negative. The rectification ratio becomes over 100 when V_{GS} is ~80 V, but the rectification ratio is just over 10 when V_{GS} range is between -40 V and -80 V. This difference in rectification ratio value is found in Figure 5c,d. Even though BD1 case current is a little higher than BD4 case current, BD2 case current is much higher than BD3 case current. It is already confirmed that the reason why BD3 case current is very small. Therefore, this big difference between two $I_{Reverse}$ current in BD2 and BD3 results in the rectification ratio value order difference in Figure 6. Thus, by using energy band diagram analysis in Figure 5, it can be understood that the reason why the rectification ratio curve in Figure 6 shows rectification ratio curve which is changed by gate voltage V_{GS}. As a result, gate-tunable rectification behavior shown in Figure 6 is understood.

2.8. Transfer I-V Curves of $PdSe_2$ Heterostructure Field Effect Transistor (Device 1)

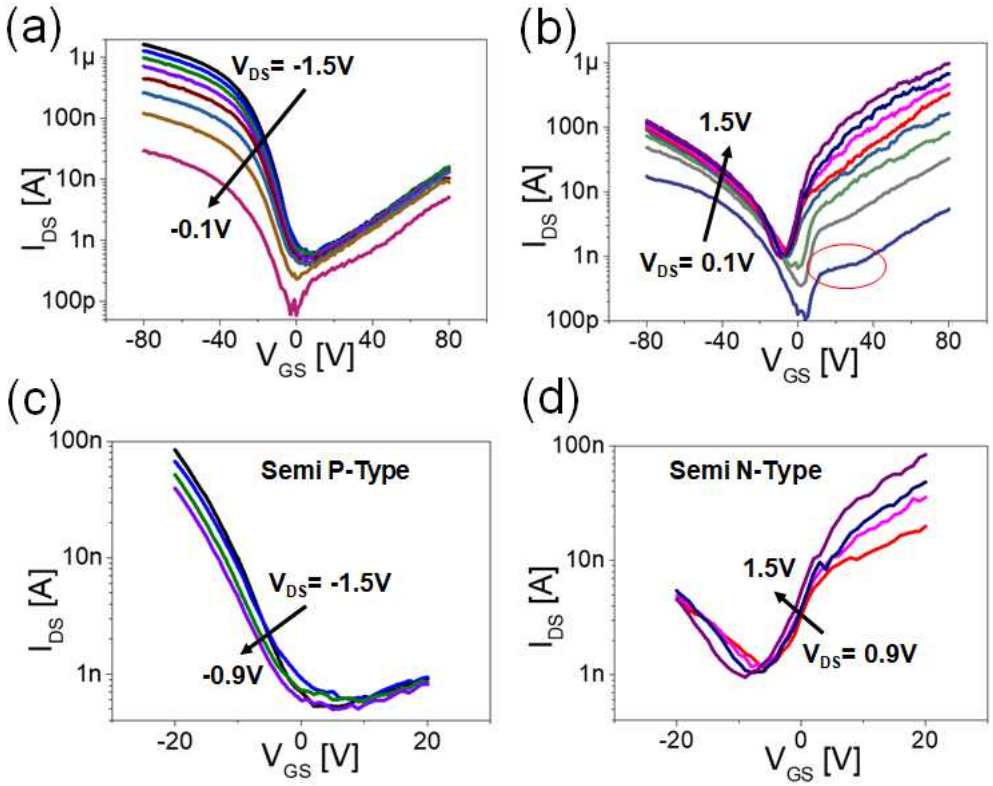


Figure 7. (a) Transfer I-V curves for Device 1 with V_{DS} from -1.5 V to -0.1 V. (b) Transfer I-V curves with V_{DS} from 0.1 V to 1.5 V. (c) Transfer I-V curves with limited V_{GS} from -20 V to 20 V and V_{DS} from -1.5 V to -0.9 V. The curves show semi p-type characteristics. (d) Transfer I-V curves with limited V_{GS} from -20 V to 20 V and V_{DS} from 0.9 V to 1.5 V. The curves show semi n-type characteristics.

Figure 7a,b show the transfer I-V curves for the $PdSe_2$ heterostructure field effect transistor (Device 1). The measured V_{GS} range is from -80 V to 80 V and V_{DS} range is from -1.5 V to 1.5 V, which is same to the voltage range in output I-V curves in Figure 5. Figure 7a shows transfer I-V curves for negative V_{DS} from -1.5 V to -0.1 V, and Figure 7b is for positive V_{DS} from 0.1 V to 1.5 V. When V_{DS} is negative, hole current level at negative V_{GS} is higher than electron current at positive V_{GS}. However, with positive V_{DS}, electron current is initially less than hole current at low V_{DS}. As V_{DS} increases, electron current increases and comparable or a little higher than hole current at V_{DS} larger than 0.9V.

Figure 7c,d are transfer I-V curves with the narrow V_{GS} and V_{DS} ranges. The limited V_{GS} range is from -20 V to 20 V and V_{DS} range is from -1.5 V to -0.9 V for Figure 7c. In Figure 7d, V_{DS} range is from 0.9

V to 1.5 V and V_{GS} range is from -20 V to 20 V. The transfer curves in Figure 7c show semi p-type characteristics. Negative V_{GS} yields higher hole current than the electron current at positive V_{GS}. Since this transfer I-V curves in Figure 7c have clear Off current at positive V_{GS}, it can be said that the I-V curves are semi p-type. In the transfer I-V curves in Figure 7d, the electron current when V_{GS} is positive is higher than the current when V_{GS} is negative. However, there is no clear Off state unlike transfer curves in Figure 7c. If limited V_{GS} range is changed to more proper range like from -10 V to 20 V, the transfer curves show clear Off state. In this work, the range is set to have 0 V in the middle. Even though electron current is increasing in negative V_{GS} range, since the current level at positive V_{GS} is higher, it can be considered as semi n-type characteristics.

From Figure 7c,d, one single $PdSe_2$ heterostructure field effect transistor can be either n- or p-type transistor. By changing V_{DS}, the transfer I-V curves can be changed to n- or p-type, which means that heterostructure $PdSe_2$ can be used to realize both n- or p-type transistor. Therefore, all PdSe2 based invert could be realized using heterostructure $PdSe_2$ [24].

2.9. Flat Region in Transfer I-V Curves and Energy Band Diagram Analysis (Device 1)

In Figure 7b, there is a flat region in transfer I-V curves when V_{DS} is 0.1 V. The red ellipse means the flat region where the transfer I-V curve's slope is not high and almost flat. Using energy band diagram analysis again, we investigate this flat region in the transfer I-V curve. Five energy band diagrams BD1 ~ BD5 are shown in in Figure 8c. In each band diagram, left side is source side and right side is drain side. Since V_{DS} is 0.1 V, the difference in energy levels for source side and drain fermi levels is small, 0.1 eV.

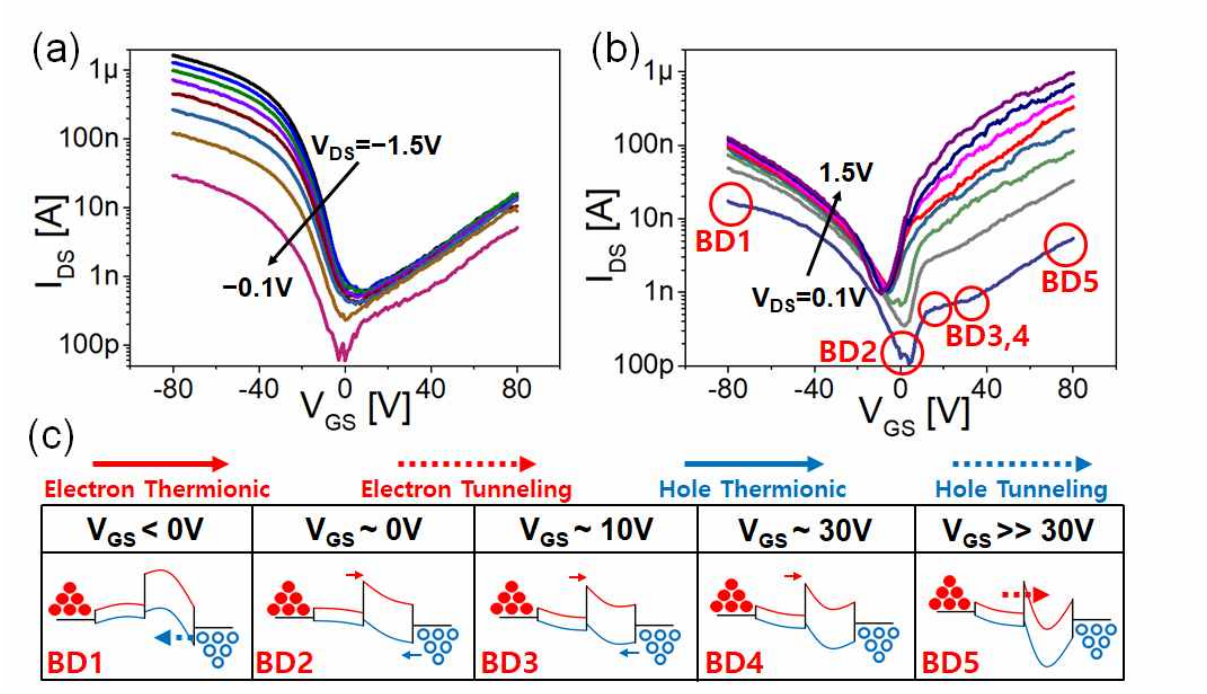


Figure 8. (a) Transfer I-V curves for Device 1 with negative V_{DS}. (b) Transfer I-V curves for Device 1 with positive V_{DS}. Five regions are chosen to analyze the flat region. (c) Energy band diagram analysis for the transfer I-V curve at V_{DS} = 0.1 V.

When V_{GS} is negative, electron current is almost negligible and there is small energy barrier for holes at drain, which results in relatively high current at BD1 in Figure 8b. When V_{GS} is ~0 V, since there are large enough energy barriers for holes and electrons respectively, the current becomes minimized, which is confirmed by BD2 in Figure 8b. As V_{GS} increases, energy band bends down. However, the amount of band bending is different for thick and think regions of $PdSe_2$ flake. If V_{GS} is less than ~10 V, electron thermionic emission current in source is mainly controlled by the height of conduction band in thin $PdSe_2$ flake which gradually decreases for increasing V_{GS}. Thus, current exponentially increases as usually observed in typical MOSFETs. When V_{GS} is between ~10 V and ~30 V, since the thick $PdSe_2$ flake has a lot of carriers, band bending is limited, and the energy band is almost fixed. Therefore, thin side energy band at the heterojunction is also fixed. Therefore, the electron thermionic emission current remains almost same. Now, as we increase V_{GS} further, energy band in thin PdSe2 flake moves down but the energy band at the heterojunction does not change much since the energy band in thick PdSe2 flake remain almost same. As a result, since total current is slowly increased, the flat region appears when V_{GS} is between ~10 V and ~30 V. However, if V_{GS} is higher than 30 V, energy band bending in thin flake becomes substantial and the tunneling barrier at the heterojunction is thinned down, thereby enhancing electron tunneling current as seen in Figure 8c BD5. Therefore, the transfer I-V curve exhibits higher slope again when V_{GS} is over ~30 V. However, this current level in BD5 case is still smaller than in BD1 case, which can be understood with BD1 and BD5 band diagrams in Figure 8c. By using this energy band diagram alignment analysis, it is understood that the reason why there is a flat region in transfer I-V curve when V_{DS} is 0.1 V and V_{GS} is between ~10 V and ~30 V.

2.10. Device Structure and Output I-V Curves of $PdSe_2$ Heterostructure Field Effect Transistor (Device 2)

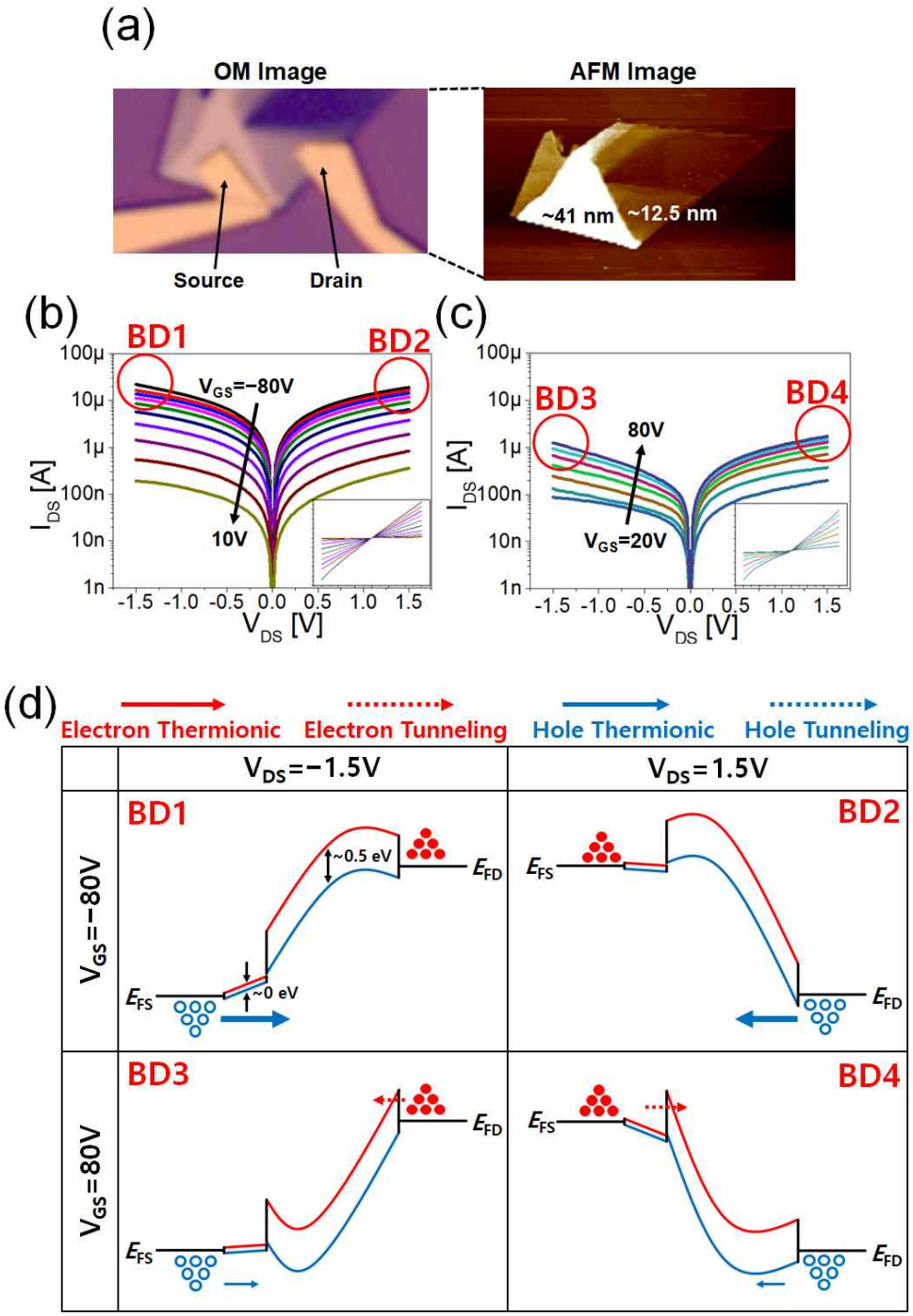


Figure 9. (a) OM and AFM images for Device 2. Heterostructure $PdSe_2$ flake is used as channel. (b) Output I-V curves for Device 2 when V_{GS} is from -80 V to 10 V. (d) Output I-V curves for Device 2 when V_{GS} is from 20 V to 80 V. (e) Energy band diagram analysis to understand the output I-V curves.

Figure 9a shows OM image and AFM image for another $PdSe_2$ heterostructure field effect transistor (Device 2). We refer again to the other study's data in Figure 5b for the information about energy band of $PdSe_2$ [23]. The thin flake part thickness is ~12.5 nm and the thick flake part thickness is ~41 nm. The corresponding number of layers is ~30 layers for thin part and ~95 layers for thick part. The corresponding energy band gap values are ~0.5 eV and ~0 eV. Using the energy values such as CBM, VBM, and band gap sizes, the four energy band diagrams are plotted in Figure 9d.

Figure 9b shows almost perfectly symmetric output I-V curves. In the inset showing I_{DS} in linear scale, it is found that the I-V curves is simply linear. In BD1 case in Figure 9d, since there is a large energy barrier for electrons at drain, the electron current is negligible. At source side, since there is almost zero energy barrier for holes, ohmic contact is formed and hence lager hole current can flow from source to drain. Therefore, we can see linear current and voltage relationship in Figure 9b BD1. In BD2 case (Figure 9d), since there is a large energy barrier for electrons at source, the electron current is negligible. At drain side, since there is very small energy barrier for holes, hole current can easily flow from drain to source by thermionic emission and tunneling. Therefore, we can see linear and sizable current in Figure 9b BD2 region. However, according to BD1 and BD2 in Figure 9d, since there is difference between energy barrier size for holes, there should be difference in the amount of hole current between BD1 case and BD2 case. The output I-V curves in Figure 9b look perfectly linear and symmetric, however, closely checking the current values reveals that BD1 case current value is a little higher than BD2 case current value. Therefore, the energy band diagram analysis is consistent to the measured output I-V curves in Figure 9b.

Figure 9c shows relatively lower current level when V_{GS} range is from 20 V to 80 V. In BD3 band diagram in Figure 9d, since there are relatively large energy barriers for both electrons and holes, total current level is smaller than the current level in Figure 9b. In BD4 band diagram in Figure 9d, since there are also relatively large energy barriers for electrons and holes respectively, total current level is smaller than the current level in Figure 9b. Since the energy barrier for electrons at source side in BD4 is lower and thinner than the energy barrier for electrons at drain side in BD3, higher current level is observed in BD4 region compared to the current level in BD3 region in Figure 9c.

The most important thing is that this $PdSe_2$ heterostructure field effect transistor (Device 2) doesn't have rectification behavior unlike Device 1, even though Device 2 also has large thickness difference between thin and thick regions. Since the thicker flake thickness is too thick ~41 nm like bulk, the corresponding band gap is ~0 eV which results in almost zero energy barrier size for carriers. Moreover, thin flake also has small band gap of ~0.5 eV. Therefore, as compared with Device 1, difference in the size of Schottky barrier height between source and drain is relatively small, which leads to negligible

current difference between DB1 and DB2. For DB3 and DB4, thick $PdSe_2$ flake has a lot of carriers which results in small band bending in energy band under the positive V_{GS}. Thus, in BD4, barrier at the heterojunction still has considerable effect even a high V_{GS}. So, the current difference between BD3 and BD4 is relatively small. As a result, for a device which has gate-tunable rectification behavior, not too thick and proper thickness of heterostructure $PdSe_2$ flake is required for the channel.

2.11. Transfer I-V Curves of $PdSe_2$ Heterostructure Field Effect Transistor (Device 2)

Figure 10 shows transfer I-V curves for the $PdSe_2$ heterostructure field effect transistor (Device 2). Figure 10a is for negative V_{DS} from -1.5 V to -0.1V and Figure 10b is for positive V_{DS} from 0.1 V to 1.5 V. In previous energy band diagram analysis in Figure 9, it is confirmed that hole current amount is much larger than electron current amount. In the transfer I-V curves in Figure 10a,b, hole current when V_{GS} is smaller than 0 V is larger than electron current when V_{GS} is higher than 0 V. Therefore, this transfer I-V curves are consistent to the energy band diagram analysis in Figure 9.

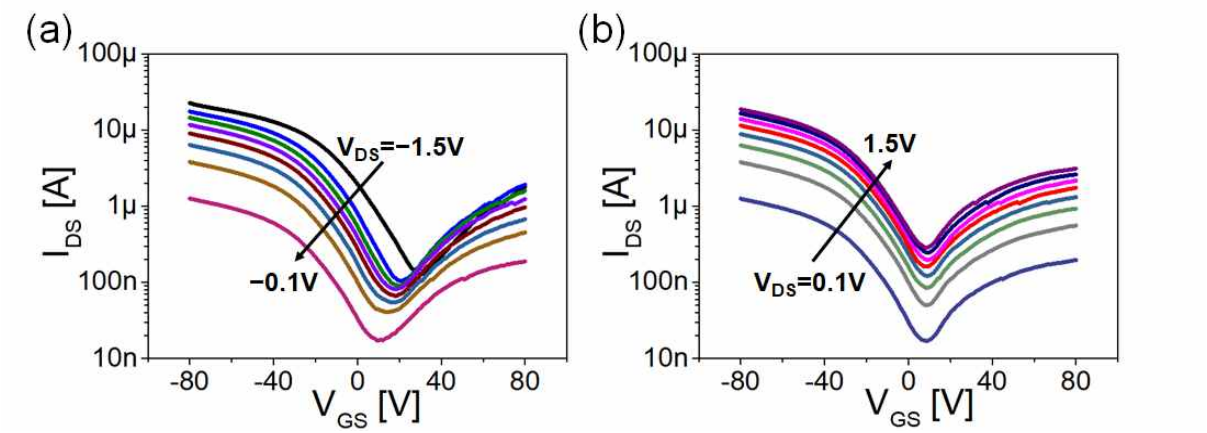


Figure 10. (a) Transfer I-V curves for Device 2 with V_{DS} from -1.5 V to -0.1 V. (b) Transfer I-V curves with V_{DS} from 0.1 V to 1.5 V. Hole current level is higher than electron current level. There is no type transition between n-type and p-type characteristics in the two I-V curve plots.

Transfer I-V curves in Figure 10 are all p-type unlike Device 1. As it is confirmed that not too thick and proper thickness $PdSe_2$ flake is required for gate-tunable rectification behavior, proper $PdSe_2$ heterostructure flake seems to be required to realize both n- and p-type transistors in the same $PdSe_2$ flake.

III. Conclusion

We study electronic band structures of monolayer, multilayer and bulk $PdSe_2$ through DFT using Atomistix Toolkit (ATK). Monolayer $PdSe_2$ has single anisotropic valleys in VB while four degenerate anisotropic valleys in CB. Calculation of band gaps for $PdSe_2$ with various thicknesses reveals clear decreasing band gap trend from ~1.1 eV (monolayer) to ~0.3 eV (Bulk).

More than 20 back-gated field effect transistors using uniform $PdSe_2$ flake as a channel are fabricated and characterized. If $PdSe_2$ flake thickness is thin enough, n-type characteristics with high On/Off ratio can be seen. As flake thickness increases, ambipolar characteristics is observed, and it becomes semi p-type if flake thickness is very thick. On and Off currents increase and the On/Off ratio decreases as $PdSe_2$ flake thickness increases. This decreasing On/Off ratio trend results from decreasing band gap trend in $PdSe_2$. Maximum mobility distribution for the fabricated uniform $PdSe_2$ devices shows that ~10 nm thickness flakes have the highest mobility value. For thin flakes, the insufficient charge screening results in the lower mobility while for thick flakes additional interlayer resistance results in the lower mobility. Therefore, the optimal thickness for higher mobility is ~10 nm.

To understand the thickness dependent transport more deeply, we fabricate other devices using heterostructure $PdSe_2$ flake as a channel. Gate-tunable rectification behavior is shown in output I-V curves for Device 1 and it is analyzed with energy band diagram analysis. Current rectification ratio curves are calculated, and behaviors of the curves are understood with the energy band diagrams. Transfer I-V curves for Device 1 shows type transition between semi n-type and semi p-type characteristics which could be used for the realization of $PdSe_2$-based inverter.

Another $PdSe_2$ heterostructure field effect transistor (Device 2) is fabricated and electrical characteristics are analyzed with the corresponding energy band diagram alignment analysis. Even though Device 2 has larger thickness difference between thin and thick parts, Device 2 doesn't have rectification behavior in output I-V curves and type transition in transfer I-V curves. These results mean that proper combination of thick and thin regions in heterostructure $PdSe_2$ flake is required for gate-tunable rectification and type transition between n-type and p-type characteristics.

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